

TLV915x-Q1 4.5MHz、轨到轨输入/输出、低失调电压、低噪声汽车级运算放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
 - 温度等级 1: -40°C 至 $+125^{\circ}\text{C}$, T_A
 - 器件 HBM ESD 分类等级 3A
 - 器件 CDM ESD 分类等级 C6
- 低失调电压: $\pm 125\mu\text{V}$
- 低失调电压漂移: $\pm 0.3\mu\text{V}/^{\circ}\text{C}$
- 低噪声: 1 kHz 时为 $10.8\text{nV}/\sqrt{\text{Hz}}$
- 高共模抑制: 120dB
- 低偏置电流: $\pm 10\text{pA}$
- 轨至轨输入和输出
- 宽带宽: 4.5MHz GBW
- 高压摆率: $21\text{V}/\mu\text{s}$
- 低静态电流: 每个放大器 $560\mu\text{A}$
- 宽电源电压: $\pm 1.35\text{V}$ 至 $\pm 8\text{V}$, 2.7V 至 16V
- 强大的 EMIRR 性能: 输入引脚上的 EMI/RFI 滤波器

2 应用

- 针对 AEC-Q100 1 级应用进行了优化
- [信息娱乐系统与仪表组](#)
- [被动安全](#)
- [车身电子装置和照明](#)
- [混合动力汽车/电动汽车逆变器和电机控制](#)
- [车载充电器 \(OBC\) 和无线充电器](#)
- [动力总成电流传感器](#)
- [高级驾驶辅助系统 \(ADAS\)](#)
- [高侧和低侧电流检测](#)

3 说明

TLV915x-Q1 系列 (TLV9151-Q1、TLV9152-Q1 和 TLV9154-Q1) 是 16V 通用汽车类运算放大器系列。这些器件具有出色的直流精度和交流性能, 包括轨到轨输出、低失调电压 ($\pm 125\mu\text{V}$, 典型值)、低温漂 ($\pm 0.3\mu\text{V}/^{\circ}\text{C}$, 典型值) 和 4.5MHz 带宽。

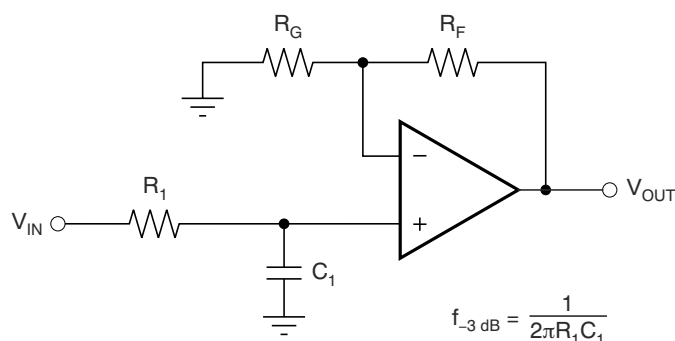
宽差分输入电压范围、高输出电流 ($\pm 75\text{mA}$)、高压摆率 ($21\text{V}/\mu\text{s}$) 以及低噪声 ($10.8\text{nV}/\sqrt{\text{Hz}}$) 等便利功能使 TLV915x-Q1 成为一款适用于汽车应用的强大的低噪声运算放大器。

TLV915x-Q1 系列运算放大器采用标准封装, 额定工作温度范围为 -40°C 至 125°C 。

器件信息

器件型号 ⁽¹⁾	封装	封装尺寸 (标称值)
TLV9151-Q1	SOT-23 (5)	2.90mm × 1.60mm
TLV9152-Q1	SOIC (8)	4.90mm × 3.90mm
	VSSOP (8)	3.00mm × 3.00mm
TLV9154-Q1	SOIC (14)	8.65mm × 3.90mm
	SOT-23 (14)	4.20mm × 1.90mm
	TSSOP (14)	5.00mm × 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

TLV915x-Q1 应用于单极低通滤波器



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (September 2021) to Revision E (March 2022) Page

• Changed maximum PSRR (2.7 V to 16 V) from $\pm 8 \mu\text{V/V}$ to $\pm 10.6 \mu\text{V/V}$	8
• Changed minimum CMRR (at 16 V) from 100 dB to 99 dB.....	8

Changes from Revision C (May 2021) to Revision D (September 2021) Page

• 删除了器件信息表中 SOIC (14) 封装的预览说明.....	1
• 删除了器件信息表中 SOT-23 (14) 封装的预览说明.....	1
• 删除了器件信息表中 SOIC (8) 封装的预览说明.....	1
• 删除了器件信息表中 SOT-23 (5) 封装的预览说明.....	1
• Deleted preview note from SOT-23 (14) package in <i>Pin Configuration and Functions</i> section.....	3
• Deleted preview note from SOIC (14) package in <i>Pin Configuration and Functions</i> section.....	3
• Deleted preview note from SOIC (8) package in <i>Pin Configuration and Functions</i> section.....	3
• Deleted preview note from SOT-23 (5) package in <i>Pin Configuration and Functions</i> section.....	3

Changes from Revision B (March 2021) to Revision C (May 2021) Page

• 删除了器件信息表中 TSSOP (14) 封装的预览说明.....	1
• Deleted preview note from TSSOP (14) package in <i>Pin Configuration and Functions</i> section.....	3
• Deleted preview note from PW package in Thermal Information for Quad Channel table.....	7

Changes from Revision A (January 2021) to Revision B (March 2021) Page

• 将器件状态从预览信息更改为生产数据.....	1
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5 Pin Configuration and Functions

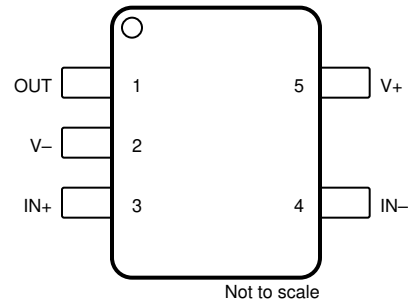
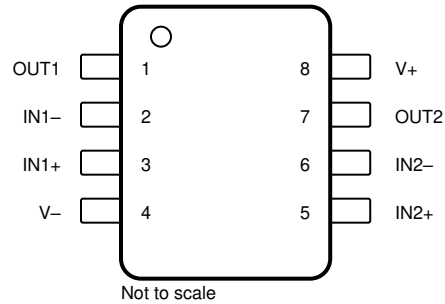


图 5-1. TLV9151-Q1 DBV Package
5-Pin SOT-23
Top View

表 5-1. Pin Functions: TLV9151-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN-	4	I	Inverting input
OUT	1	O	Output
V+	5	—	Positive (highest) power supply
V-	2	—	Negative (lowest) power supply



**图 5-2. TLV9152-Q1 D and DGK Package
8-Pin SOIC and VSSOP
Top View**

表 5-2. Pin Functions: TLV9152-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN1–	2	I	Inverting input, channel 1
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply



**图 5-3. TLV9154-Q1 D, DYY, and PW Package
14-Pin SOIC, SOT-23, and TSSOP
Top View**

表 5-3. Pin Functions: TLV9154-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1-	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2-	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3-	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4-	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V-	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	20	V
Signal input pins	Common-mode voltage ⁽³⁾	$(V-) - 0.5$	$(V+) + 0.5$	V
	Differential voltage ⁽³⁾		$V_S + 0.2$	V
	Current ⁽³⁾	-10	10	mA
Output short-circuit ⁽²⁾		Continuous		
Operating ambient temperature, T_A		-55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- Short-circuit to ground, one amplifier per package.
- Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, $(V+) - (V-)$	2.7	16	V
V_I	Input voltage range	$(V-) - 0.1$	$(V+) + 0.1$	V
T_A	Specified ambient temperature	-40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC ⁽¹⁾		TLV9151-Q1	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Thermal Information for Dual Channel

THERMAL METRIC ⁽¹⁾		TLV9152-Q1		Unit
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	132.6	176.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	73.4	68.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	76.1	98.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	24.0	12.0	°C/W
ψ _{JB}	Junction-to-board characterization parameter	75.4	96.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.6 Thermal Information for Quad Channel

THERMAL METRIC ⁽¹⁾		TLV9154-Q1			UNIT
		D (SOIC)	DYY (SOT-23)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	101.4	110.7	118.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	57.6	55.9	47.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	57.3	35.3	60.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	18.5	2.3	6.0	°C/W
ψ _{JB}	Junction-to-board characterization parameter	56.9	35.1	60.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.7 Electrical Characteristics

For $V_S = (V+) - (V-) = 2.7\text{ V to }16\text{ V}$ ($\pm 1.35\text{ V to } \pm 8\text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O\text{ UT}} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	$V_{CM} = V-$			± 125	± 895	μV
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$			± 925	
dV_{OS}/dT	Input offset voltage drift		$T_A = -40^\circ\text{C to }125^\circ\text{C}$		± 0.3		$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage versus power supply	$V_{CM} = V-, V_S = 4\text{ V to }16\text{ V}$	$T_A = -40^\circ\text{C to }125^\circ\text{C}$		± 0.3	± 1.5	$\mu\text{V/V}$
		$V_{CM} = V-, V_S = 2.7\text{ V to }16\text{ V}^{(2)}$			± 1	± 10.6	
	Channel separation	$f = 0\text{ Hz}$			5		$\mu\text{V/V}$
INPUT BIAS CURRENT							
I_B	Input bias current				± 10		pA
			$T_A = -40^\circ\text{C to }125^\circ\text{C}^{(2)}$			± 1	nA
I_{OS}	Input offset current				± 10		pA
			$T_A = -40^\circ\text{C to }125^\circ\text{C}^{(2)}$			± 1	nA
NOISE							
E_N	Input voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$			1.8		μV_{PP}
					0.3		μV_{RMS}
e_N	Input voltage noise density	$f = 1\text{ kHz}$			10.8		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$			9.4		
i_N	Input current noise	$f = 1\text{ kHz}$			2		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			$(V-) - 0.1$		$(V+) + 0.1$	V
CMRR	Common-mode rejection ratio	$V_S = 16\text{ V}, (V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$ (Main input pair)	$T_A = -40^\circ\text{C to }125^\circ\text{C}$		99	130	dB
		$V_S = 4\text{ V}, (V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$ (Main input pair)			82	100	
		$V_S = 2.7\text{ V}, (V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$ (Main input pair) ⁽²⁾			75	95	
		$V_S = 2.7\text{ V to }16\text{ V}, (V+) - 1\text{ V} < V_{CM} < (V+) + 0.1\text{ V}$ (Aux input pair)				85	
INPUT CAPACITANCE							
Z_{ID}	Differential				100 9		$\text{M}\Omega \text{pF}$
Z_{ICM}	Common-mode				6 1		$\text{T}\Omega \text{pF}$
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	$V_S = 16\text{ V}, V_{CM} = V- (V-) + 0.1\text{ V} < V_O < (V+) - 0.1\text{ V}$	$T_A = -40^\circ\text{C to }125^\circ\text{C}$		120	145	dB
					142		
		$V_S = 4\text{ V}, V_{CM} = V- (V-) + 0.1\text{ V} < V_O < (V+) - 0.1\text{ V}$	$T_A = -40^\circ\text{C to }125^\circ\text{C}$		104	130	
					125		
	$V_S = 2.7\text{ V}, V_{CM} = V- (V-) + 0.1\text{ V} < V_O < (V+) - 0.1\text{ V}^{(2)}$	$T_A = -40^\circ\text{C to }125^\circ\text{C}$		101	120		
				118			

6.7 Electrical Characteristics (continued)

For $V_S = (V+) - (V-) = 2.7\text{ V to }16\text{ V}$ ($\pm 1.35\text{ V to } \pm 8\text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			4.5		MHz
SR	Slew rate	$V_S = 16\text{ V}$, $G = +1$, $C_L = 20\text{ pF}$		21		V/ μs
t_s	Settling time	To 0.01%, $V_S = 16\text{ V}$, $V_{STEP} = 10\text{ V}$, $G = +1$, $C_L = 20\text{ pF}$		2.5		μs
		To 0.01%, $V_S = 16\text{ V}$, $V_{STEP} = 2\text{ V}$, $G = +1$, $C_L = 20\text{ pF}$		1.5		
		To 0.1%, $V_S = 16\text{ V}$, $V_{STEP} = 10\text{ V}$, $G = +1$, $C_L = 20\text{ pF}$		2		
		To 0.1%, $V_S = 16\text{ V}$, $V_{STEP} = 2\text{ V}$, $G = +1$, $C_L = 20\text{ pF}$		1		
	Phase margin	$G = +1$, $R_L = 10\text{ k}\Omega$		60		$^\circ$
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$		400		ns
THD+N	Total harmonic distortion + noise ⁽¹⁾	$V_S = 16\text{ V}$, $V_O = 3 V_{RMS}$, $G = 1$, $f = 1\text{ kHz}$		0.00021%		
OUTPUT						
	Voltage output swing from rail (positive and negative)	$V_S = 16\text{ V}$, $R_L = \text{no load}$		5	10	mV
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$ ⁽²⁾		15	
		$V_S = 16\text{ V}$, $R_L = 10\text{ k}\Omega$		50	55	
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$ ⁽²⁾		75	
		$V_S = 16\text{ V}$, $R_L = 2\text{ k}\Omega$		200	250	
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$ ⁽²⁾		350	
		$V_S = 2.7\text{ V}$, $R_L = \text{no load}$		1	6	
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$ ⁽²⁾		10	
$V_S = 2.7\text{ V}$, $R_L = 10\text{ k}\Omega$		5	12			
	$T_A = -40^\circ\text{C to }125^\circ\text{C}$ ⁽²⁾		18			
$V_S = 2.7\text{ V}$, $R_L = 2\text{ k}\Omega$		25	40			
	$T_A = -40^\circ\text{C to }125^\circ\text{C}$ ⁽²⁾		60			
I_{SC}	Short-circuit current			± 75		mA
C_{LOAD}	Capacitive load drive			1000		pF
Z_O	Open-loop output impedance	$f = 1\text{ MHz}$, $I_O = 0\text{ A}$		525		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	$I_O = 0\text{ A}$		560	685	μA
		$I_O = 0\text{ A}$, (TLV9151-Q1)		560	691	
		$I_O = 0\text{ A}$	$T_A = -40^\circ\text{C to }125^\circ\text{C}$		750	
		$I_O = 0\text{ A}$, (TLV9151-Q1)			769	

(1) Third-order filter; bandwidth = 80 kHz at -3 dB.

(2) Specified by characterization only.

6.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{ pF}$ (unless otherwise noted)

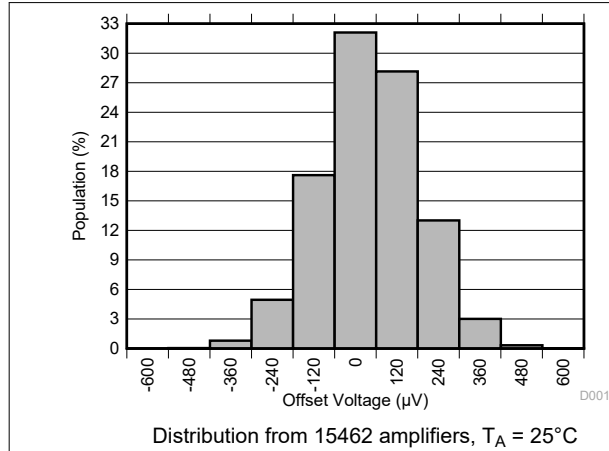


图 6-1. Offset Voltage Production Distribution

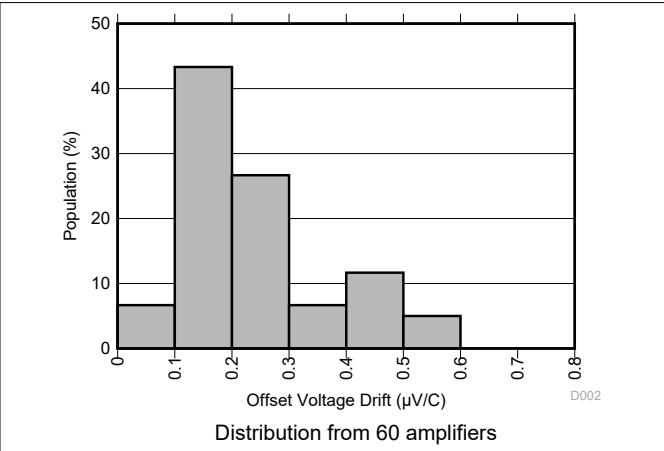


图 6-2. Offset Voltage Drift Distribution

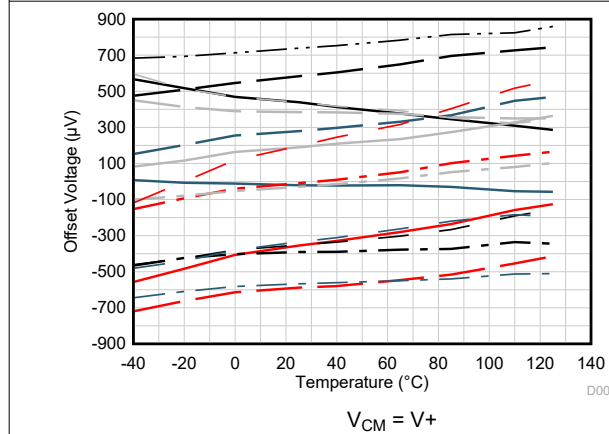


图 6-3. Offset Voltage vs Temperature

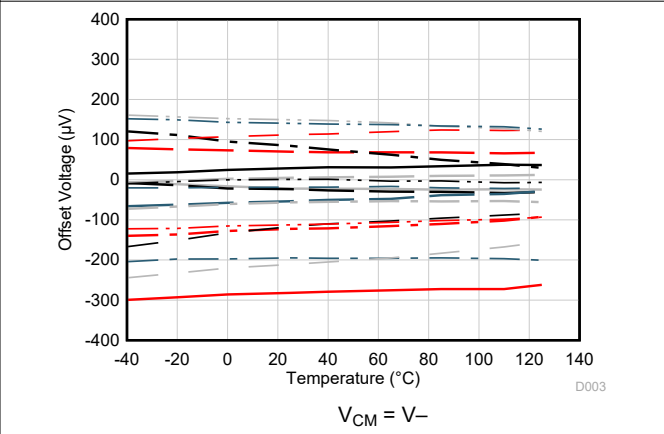


图 6-4. Offset Voltage vs Temperature

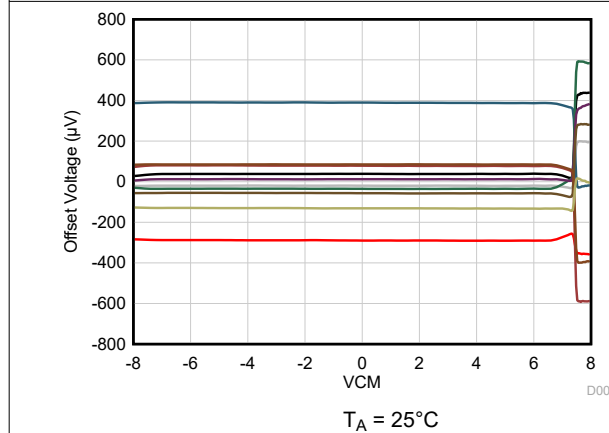


图 6-5. Offset Voltage vs Common-Mode Voltage

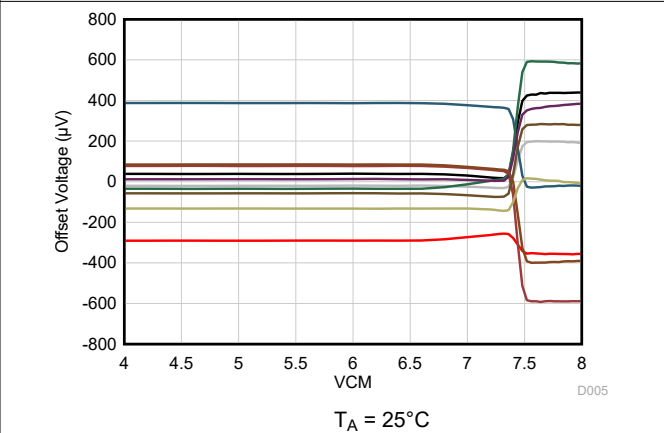


图 6-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{ pF}$ (unless otherwise noted)

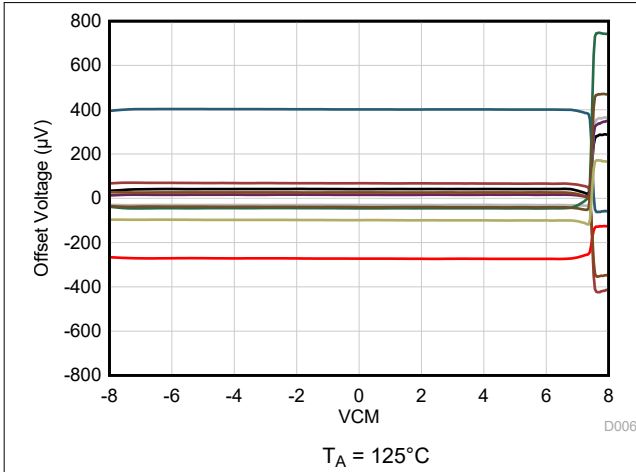


图 6-7. Offset Voltage vs Common-Mode Voltage

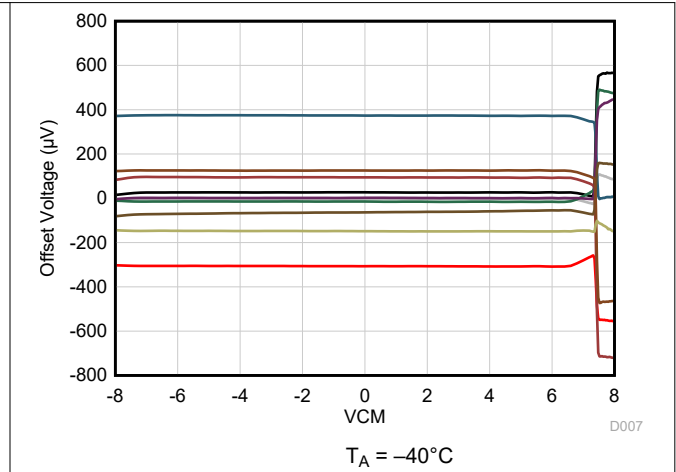


图 6-8. Offset Voltage vs Common-Mode Voltage

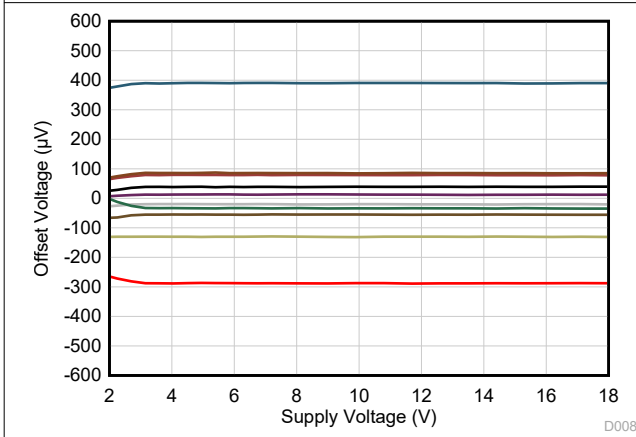


图 6-9. Offset Voltage vs Power Supply

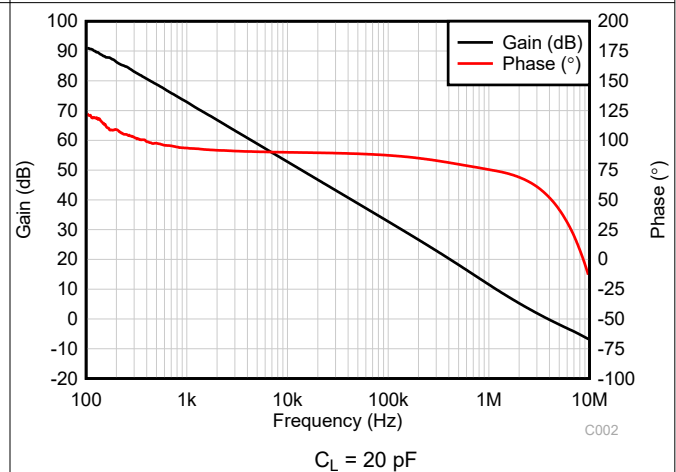


图 6-10. Open-Loop Gain and Phase vs Frequency

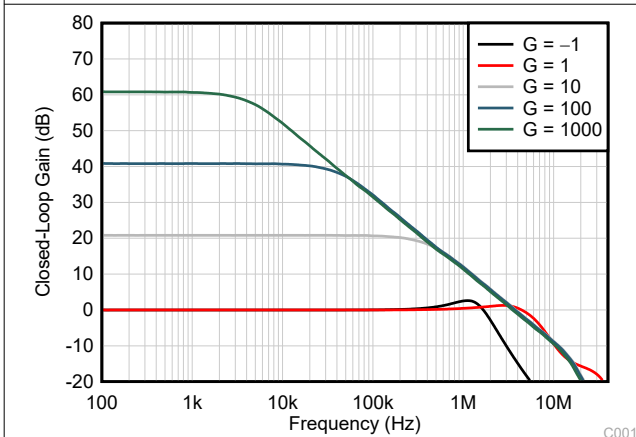


图 6-11. Closed-Loop Gain vs Frequency

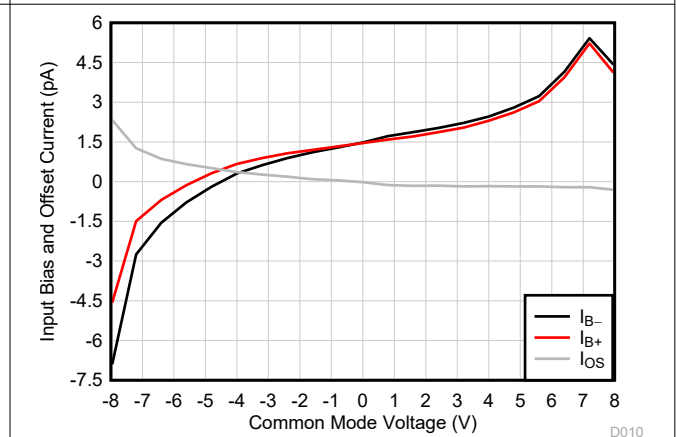


图 6-12. Input Bias Current vs Common-Mode Voltage

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{ pF}$ (unless otherwise noted)

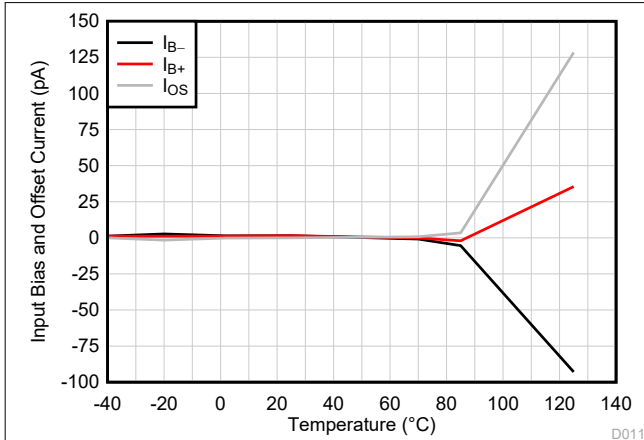


图 6-13. Input Bias Current vs Temperature

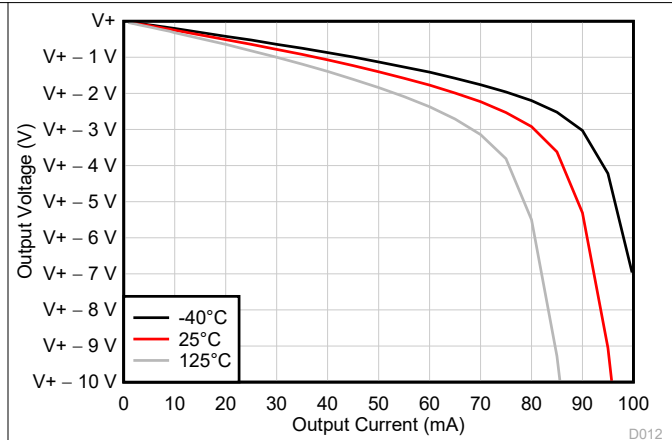


图 6-14. Output Voltage Swing vs Output Current (Sourcing)

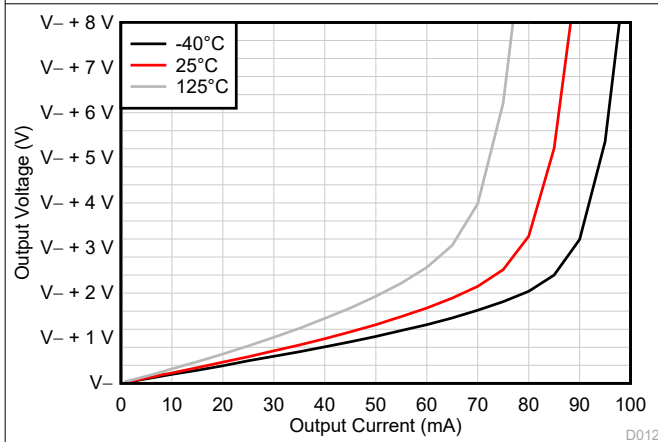


图 6-15. Output Voltage Swing vs Output Current (Sinking)

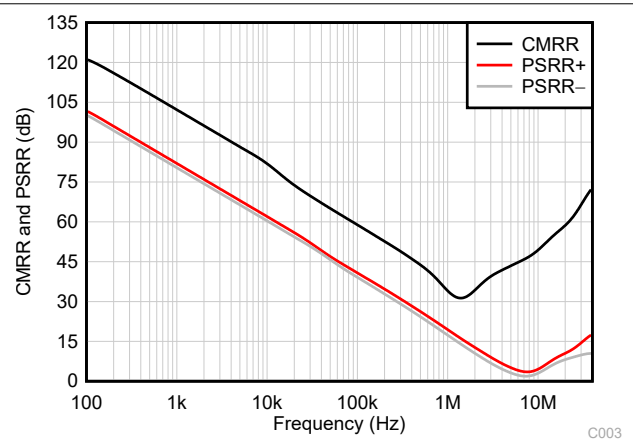


图 6-16. CMRR and PSRR vs Frequency

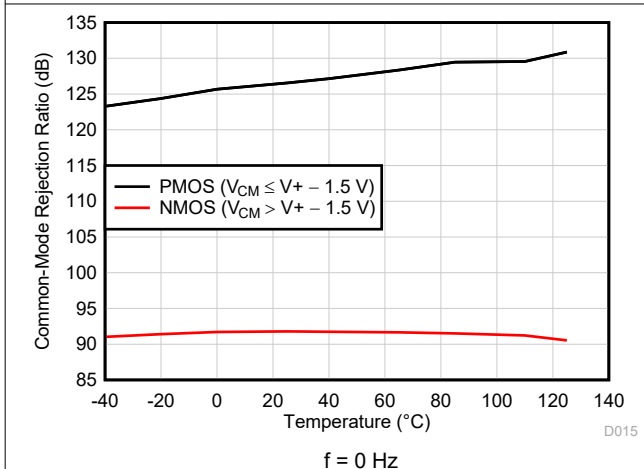


图 6-17. CMRR vs Temperature (dB)

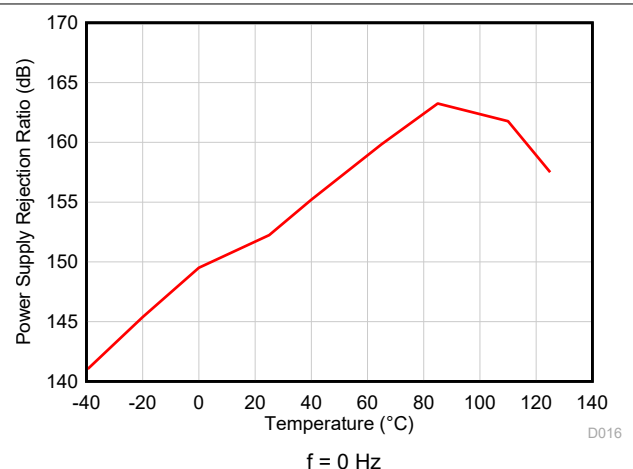


图 6-18. PSRR vs Temperature (dB)

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{ pF}$ (unless otherwise noted)

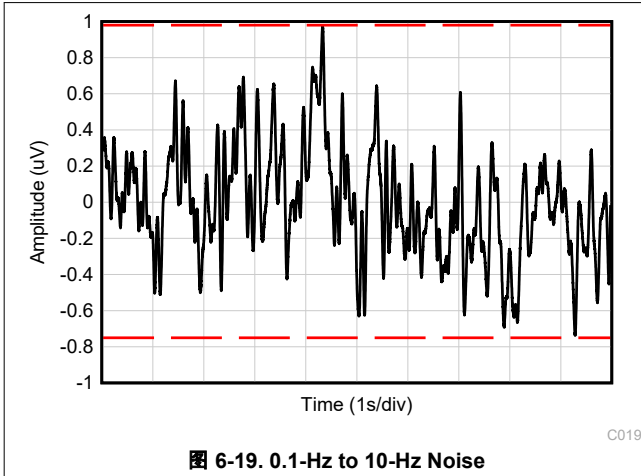


图 6-19. 0.1-Hz to 10-Hz Noise

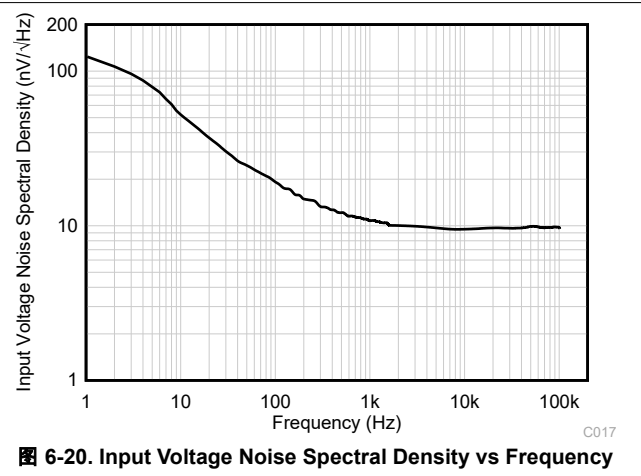


图 6-20. Input Voltage Noise Spectral Density vs Frequency

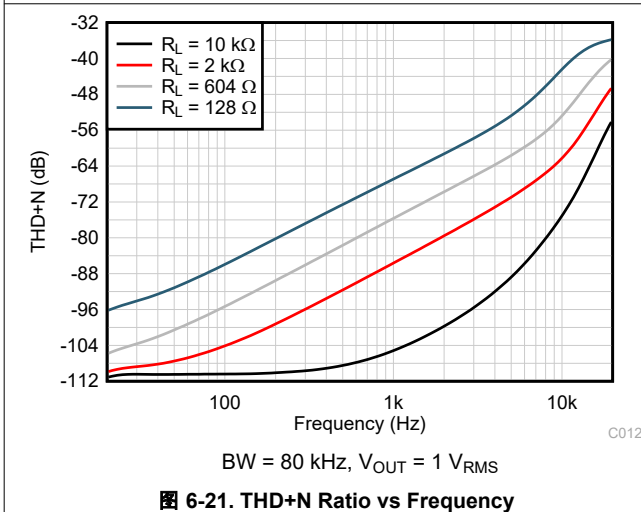


图 6-21. THD+N Ratio vs Frequency

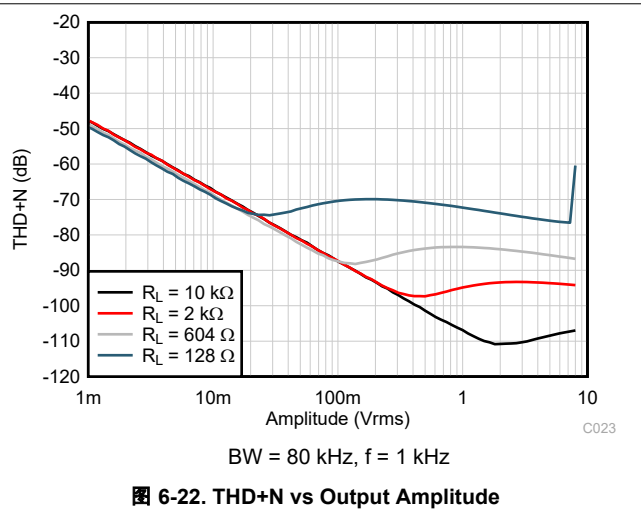


图 6-22. THD+N vs Output Amplitude

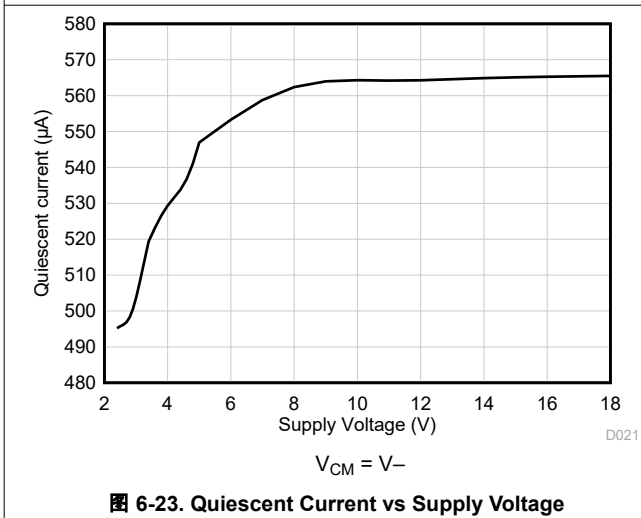


图 6-23. Quiescent Current vs Supply Voltage

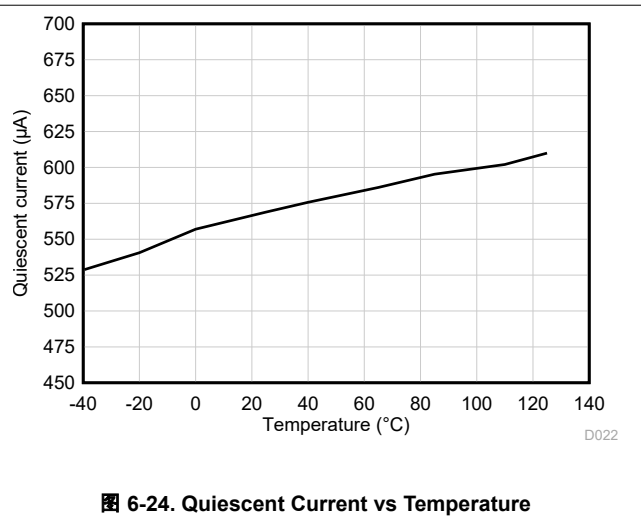


图 6-24. Quiescent Current vs Temperature

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{ pF}$ (unless otherwise noted)

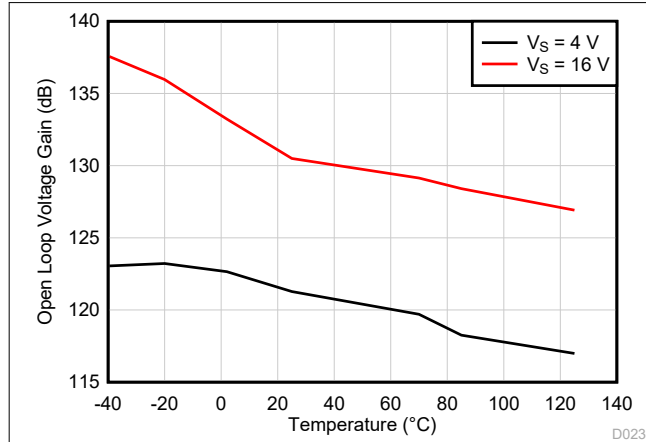


图 6-25. Open-Loop Voltage Gain vs Temperature (dB)

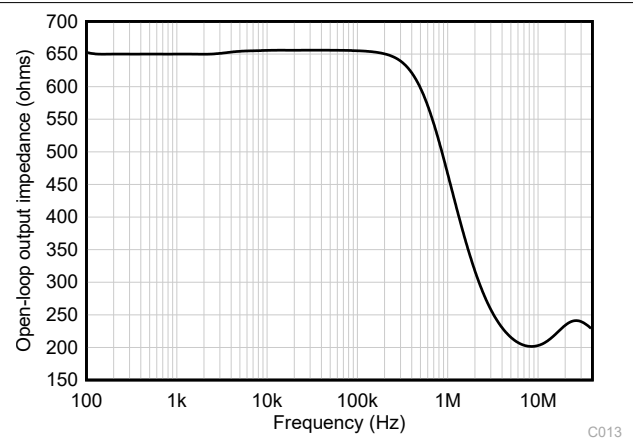


图 6-26. Open-Loop Output Impedance vs Frequency

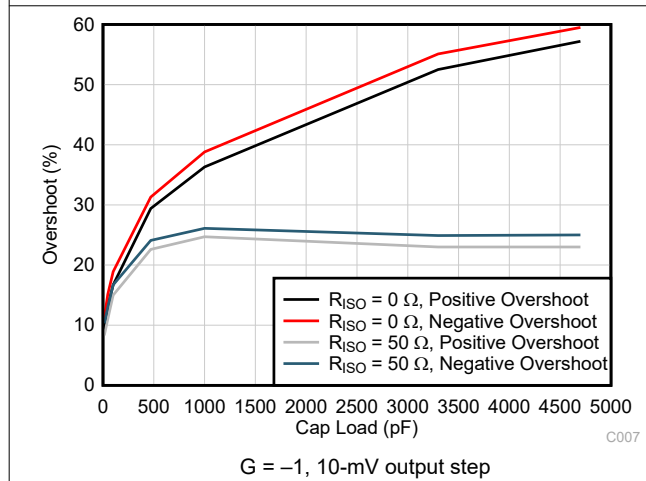


图 6-27. Small-Signal Overshoot vs Capacitive Load

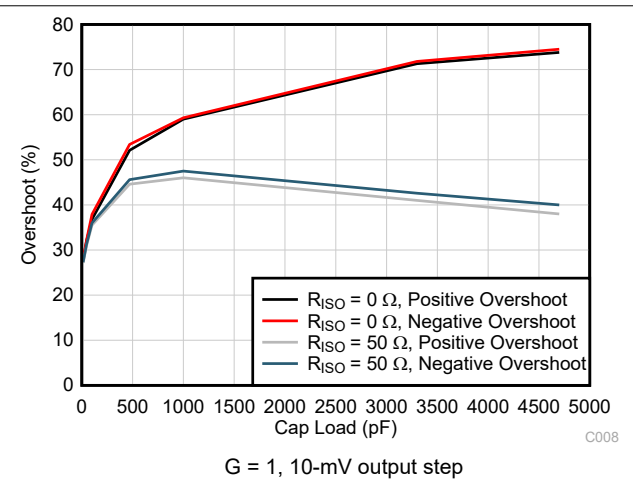


图 6-28. Small-Signal Overshoot vs Capacitive Load

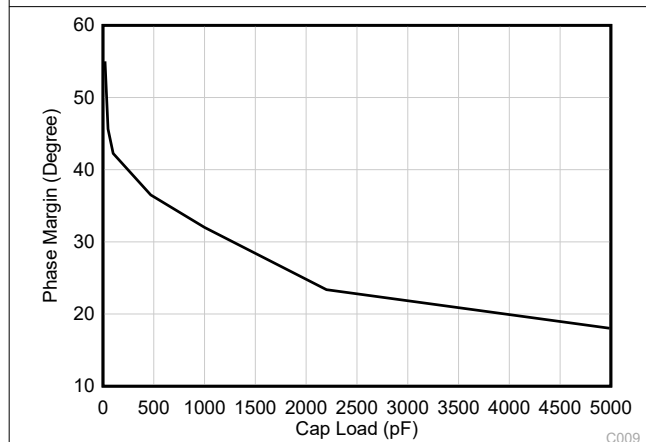


图 6-29. Phase Margin vs Capacitive Load

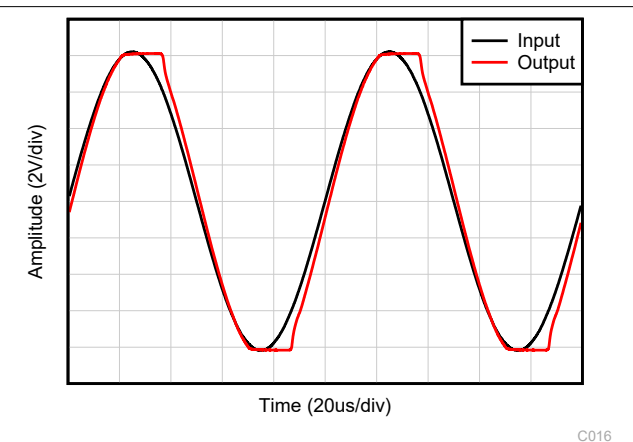
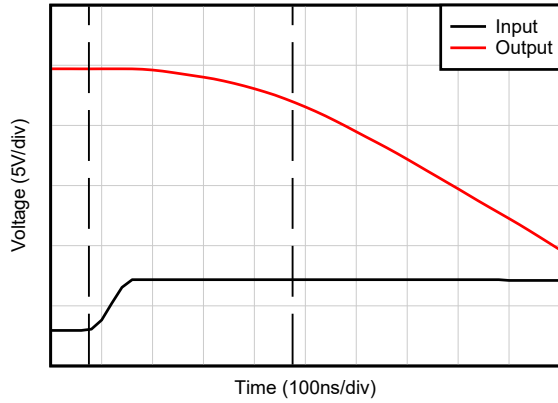


图 6-30. No Phase Reversal

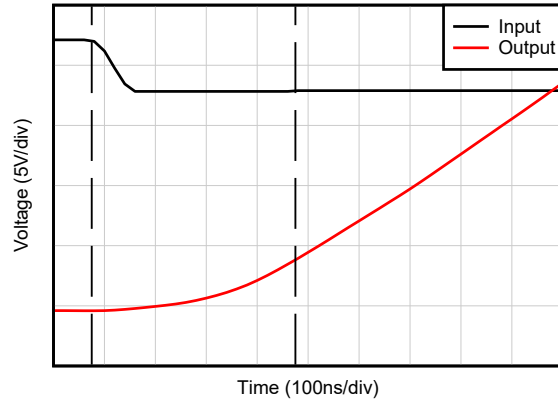
6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{ pF}$ (unless otherwise noted)



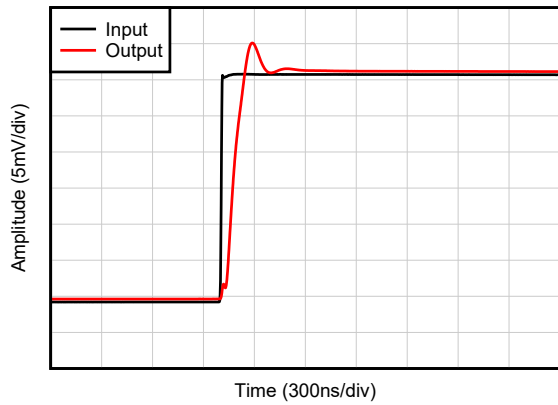
$G = -10$

图 6-31. Positive Overload Recovery



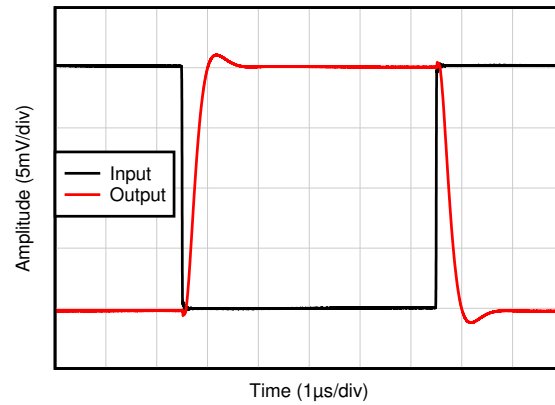
$G = -10$

图 6-32. Negative Overload Recovery



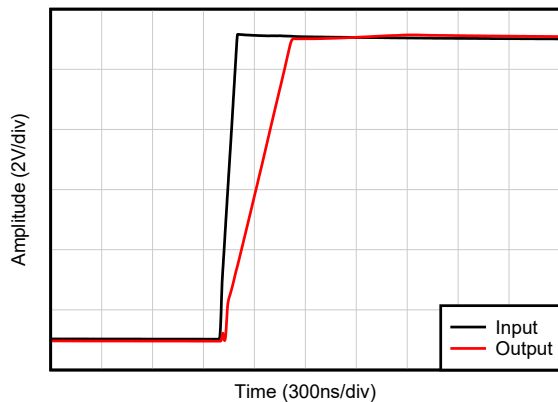
$C_L = 20\text{ pF}$, $G = 1$, 20-mV step response

图 6-33. Small-Signal Step Response, Rising



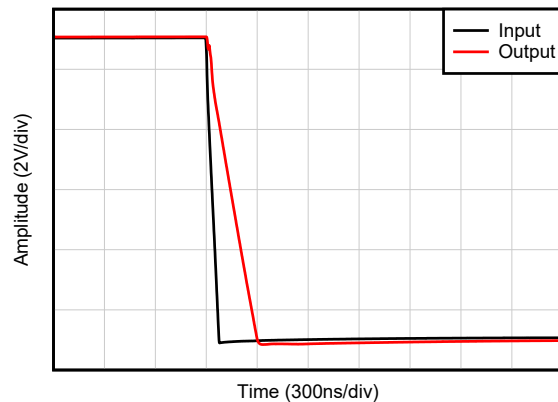
$C_L = 20\text{ pF}$, $G = -1$, 20-mV step response

图 6-34. Small-Signal Step Response



$C_L = 20\text{ pF}$, $G = 1$

图 6-35. Large-Signal Step Response (Rising)



$C_L = 20\text{ pF}$, $G = 1$

图 6-36. Large-Signal Step Response (Falling)

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{ pF}$ (unless otherwise noted)

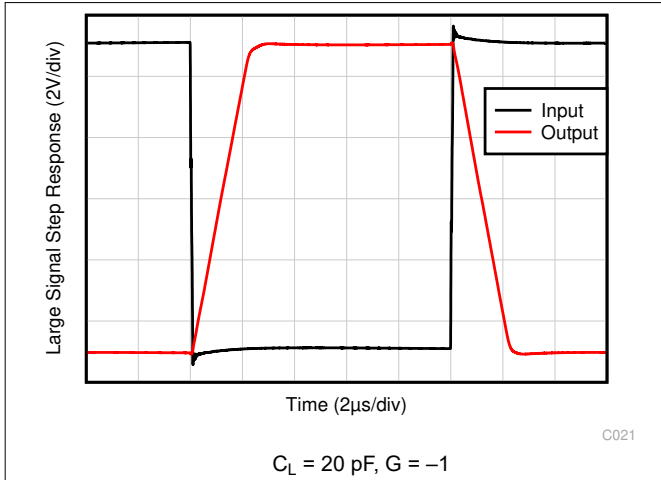


图 6-37. Large-Signal Step Response

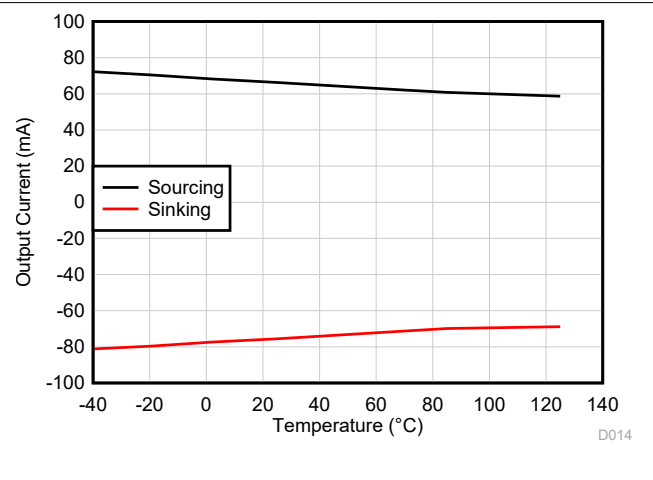


图 6-38. Short-Circuit Current vs Temperature

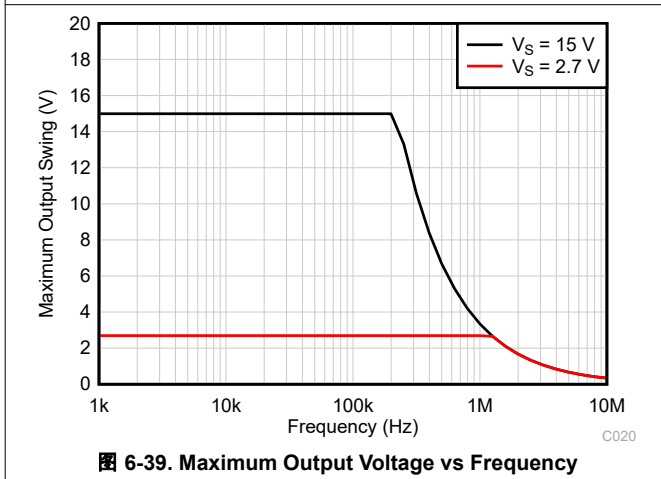


图 6-39. Maximum Output Voltage vs Frequency

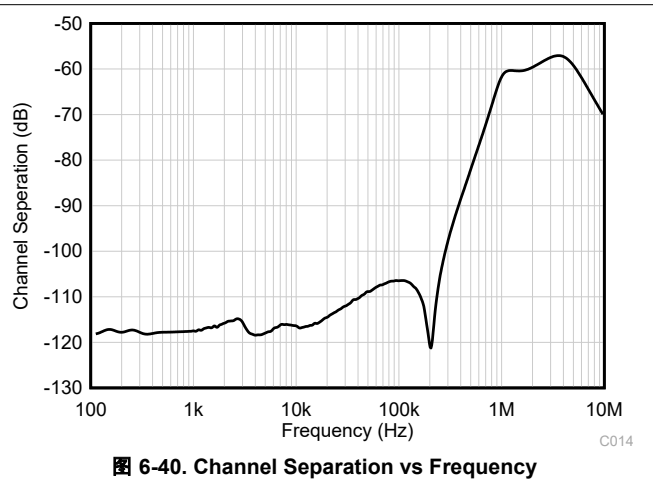


图 6-40. Channel Separation vs Frequency

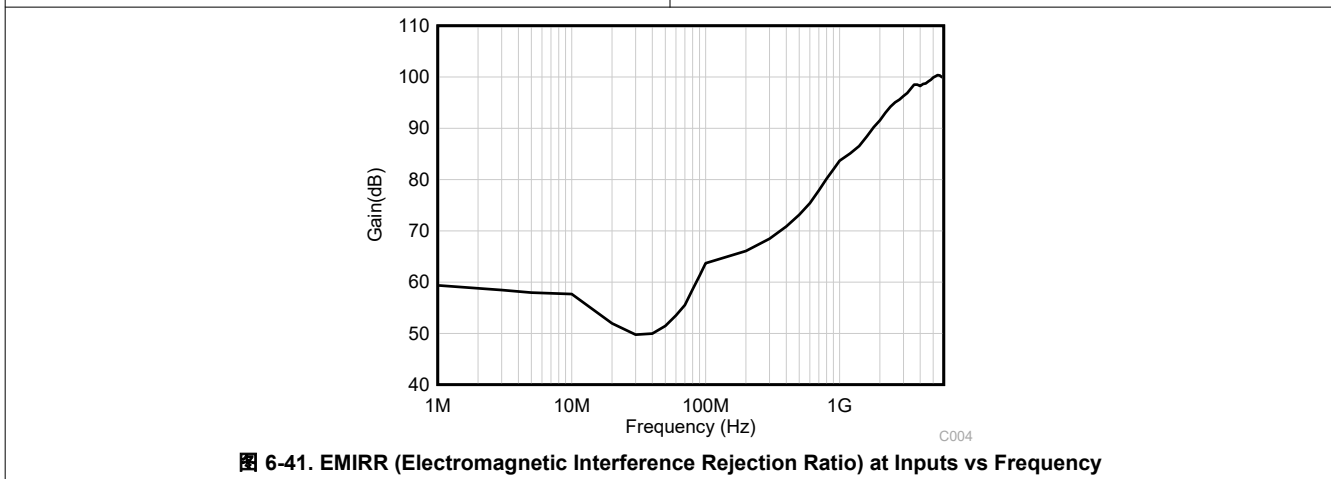


图 6-41. EMIRR (Electromagnetic Interference Rejection Ratio) at Inputs vs Frequency

7 Detailed Description

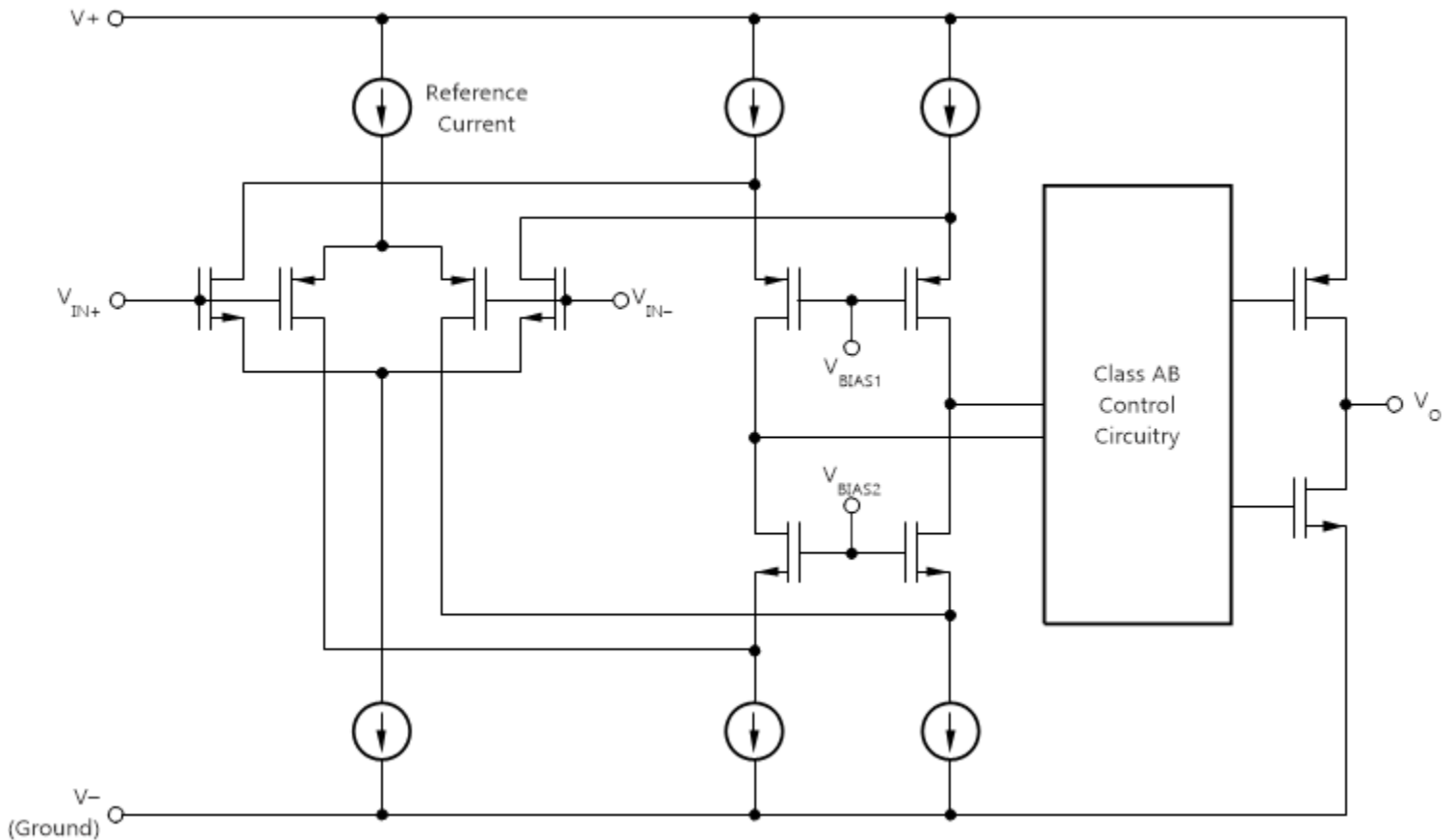
7.1 Overview

The TLV915x-Q1 family (TLV9151-Q1, TLV9152-Q1, and TLV9154-Q1) is a family of 16-V general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset ($\pm 125 \mu\text{V}$, typ), low offset drift ($\pm 0.3 \mu\text{V}/^\circ\text{C}$, typ), and 4.5-MHz bandwidth.

Wide differential and common-mode input-voltage range, high output current ($\pm 75 \text{ mA}$), high slew rate (21 $\text{V}/\mu\text{s}$), and low power operation (560 μA , typ) make the TLV915x-Q1 a robust, high-speed, high-performance operational amplifier for industrial applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 EMI Rejection

The TLV915x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV915x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 7-1 shows the results of this testing on the TLV915x-Q1. 表 7-1 shows the EMIRR IN+ values for the TLV915x-Q1 at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational Amplifiers](#) application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

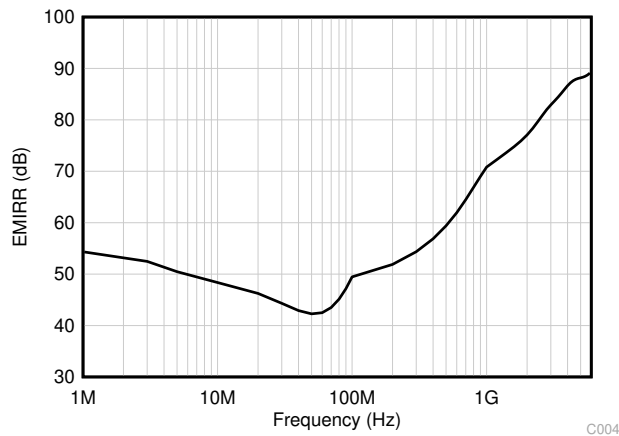


图 7-1. EMIRR Testing

表 7-1. TLV915x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	87.6 dB

7.3.2 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV915x-Q1 is 150°C. Exceeding this temperature causes damage to the device. The TLV915x-Q1 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 图 7-2 shows an application example for the TLV9151-Q1 that has significant self heating because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature will reach 177°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 图 7-2 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L . If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.

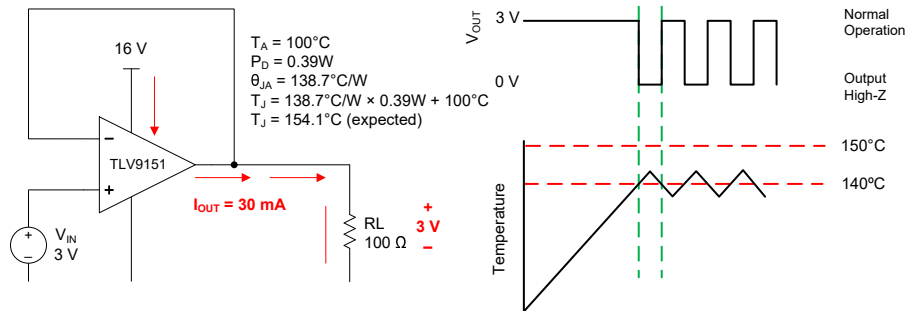


图 7-2. Thermal Protection

7.3.3 Capacitive Load and Stability

The TLV915x-Q1 features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 7-3 and 图 7-4. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

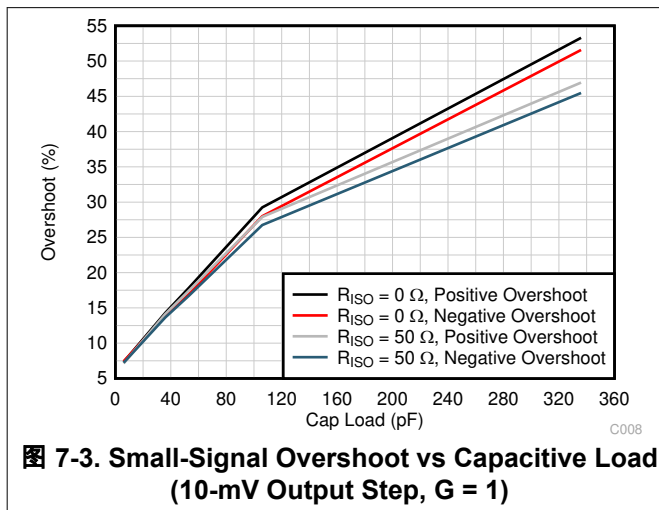


图 7-3. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = 1)

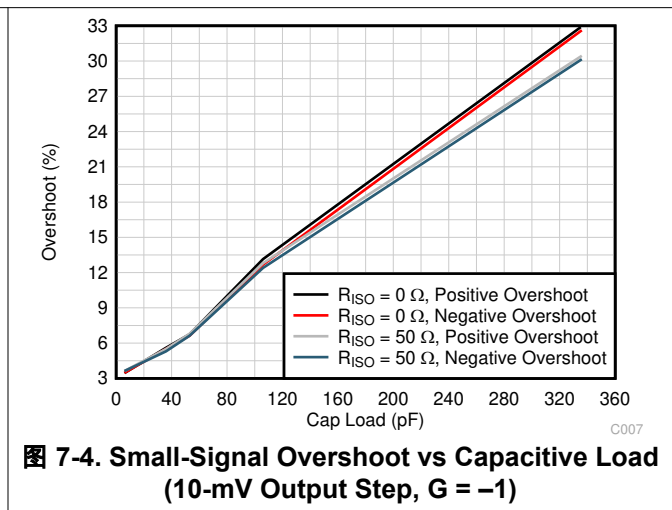


图 7-4. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = -1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO} , in series with the output, as shown in 图 7-5. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the

capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L , and is generally negligible at low output levels. A high capacitive load drive makes the TLV915x-Q1 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in [图 7-5](#) uses an isolation resistor, R_{ISO} , to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

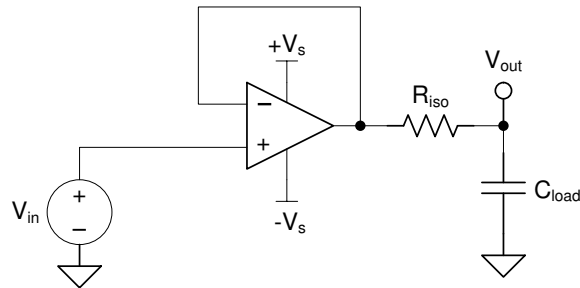


图 7-5. Extending Capacitive Load Drive With the TLV9151-Q1

7.3.4 Common-Mode Voltage Range

The TLV915x-Q1 is a 16-V, rail-to-rail input operational amplifier with an input common-mode range that extends 200 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in [图 7-6](#). The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1\text{ V}$ to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately $(V+) - 2\text{ V}$. There is a small transition region, typically $(V+) - 2\text{ V}$ to $(V+) - 1\text{ V}$ in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

[图 6-5](#) shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see [Op Amps With Complementary-Pair Input Stages](#) application note.

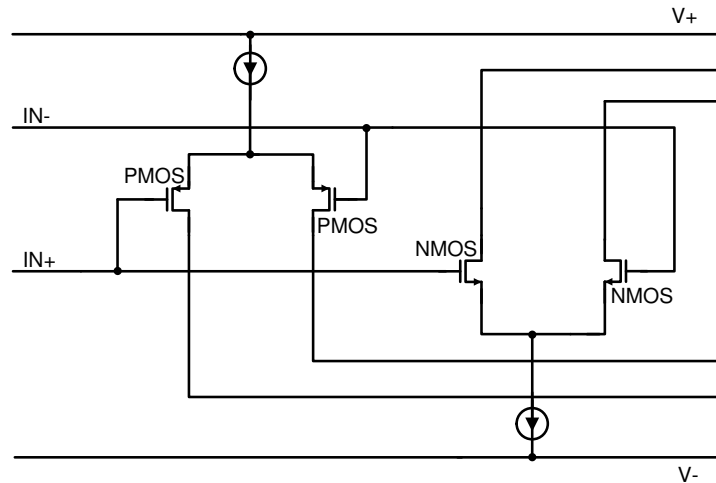


图 7-6. Rail-to-Rail Input Stage

7.3.5 Phase Reversal Protection

The TLV915x-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV915x-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in [图 7-7](#). For more information on phase reversal, see [Op Amps With Complementary-Pair Input Stages](#) application note.

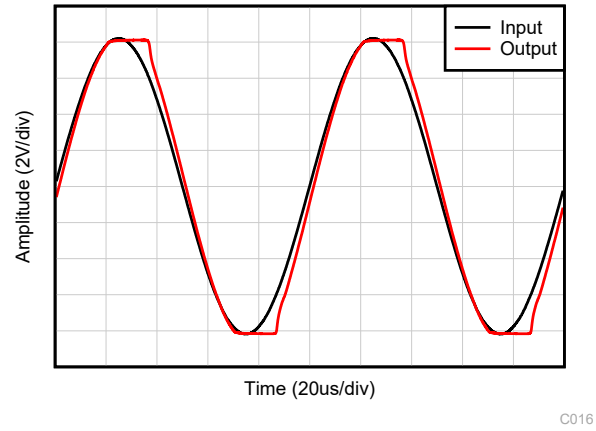


图 7-7. No Phase Reversal

7.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 7-8 shows an illustration of the ESD circuits contained in the TLV915x-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

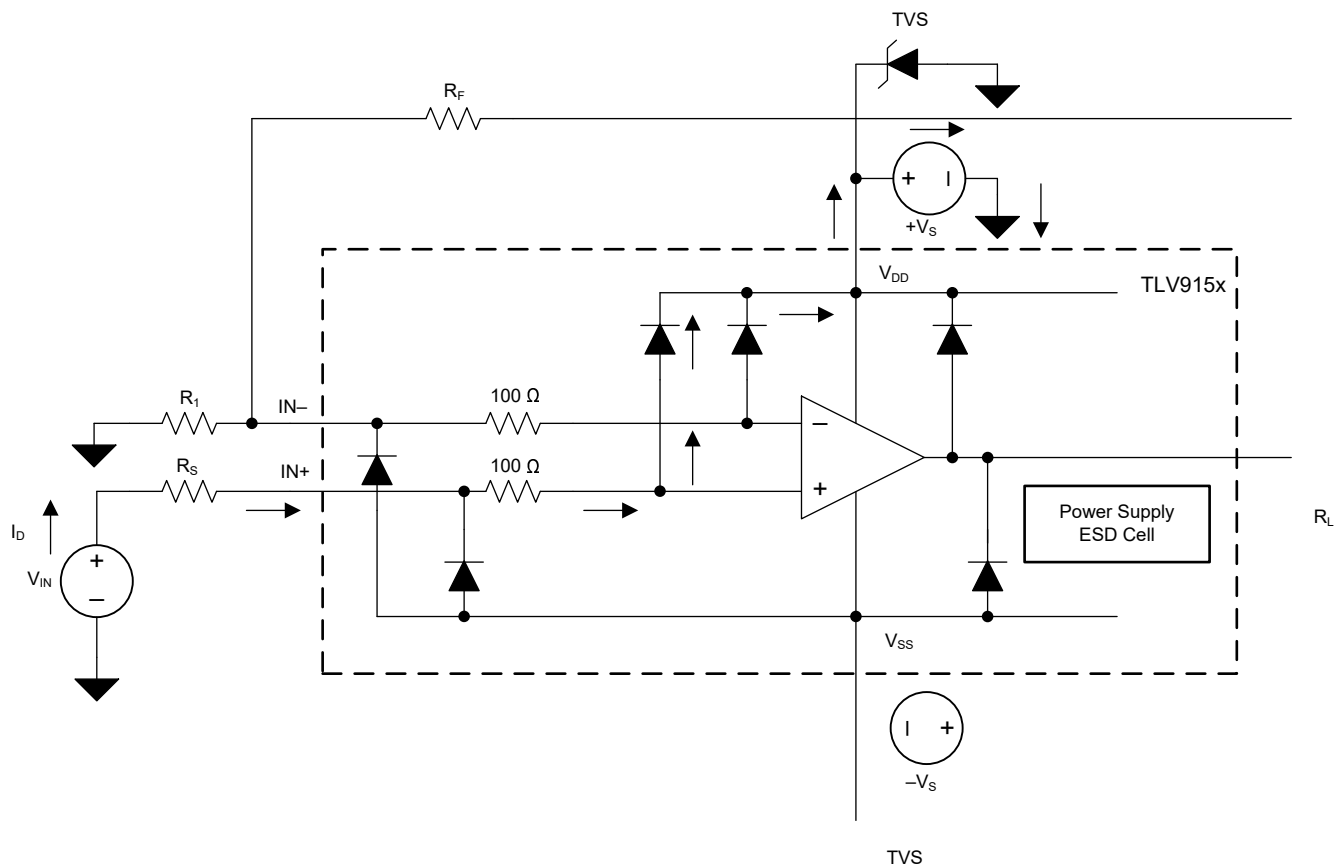


图 7-8. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.7 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV915x-Q1 is approximately 400 ns.

7.3.8 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in [§ 6.7](#).

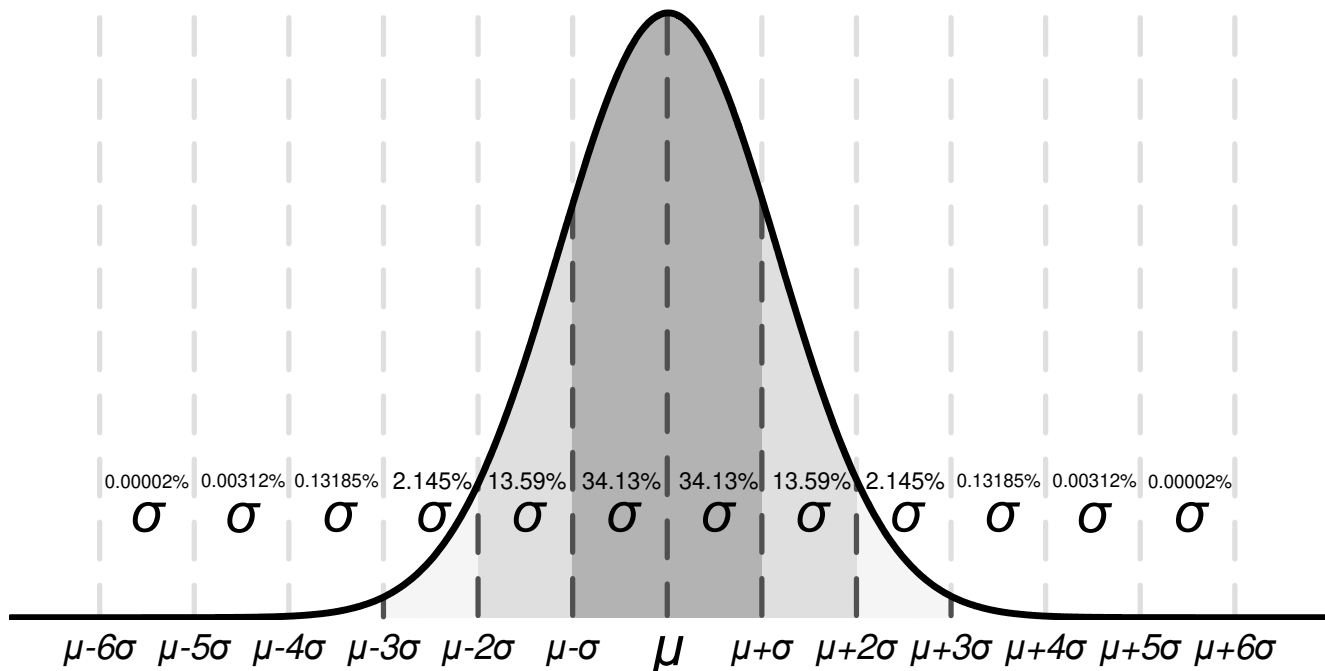


图 7-9. Ideal Gaussian Distribution

图 7-9 shows an example distribution, where μ , or *mu*, is the mean of the distribution, and where σ , or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of [§ 6.7](#) are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation ($\mu + \sigma$) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for TLV915x-Q1, the typical input voltage offset is 125 μV , so 68.2% of all TLV915x-Q1 devices are expected to have an offset from $-125 \mu\text{V}$ to $125 \mu\text{V}$. At 4σ ($\pm 500 \mu\text{V}$), 99.9937% of the distribution has an offset voltage less than

$\pm 500 \mu\text{V}$, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV915x-Q1 family has a maximum offset voltage of $675 \mu\text{V}$ at 25°C , and even though this corresponds to about 5σ (≈ 1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than $895 \mu\text{V}$ will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the $6\text{-}\sigma$ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV915x-Q1 family does not have a maximum or minimum for offset voltage drift, but based on [Figure 6-2](#) and the typical value of $0.3 \mu\text{V}/^\circ\text{C}$ in [Section 6.7](#), it can be calculated that the $6\text{-}\sigma$ value for offset voltage drift is about $1.8 \mu\text{V}/^\circ\text{C}$. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

7.3.9 Packages With an Exposed Thermal Pad

The TLV915x-Q1 family is available in packages such as the WSON-8 (DSG) and WQFN-16 (RTE) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to $V-$ or left floating. Attaching the thermal pad to a potential other than $V-$ is not allowed, and performance of the device is not assured when doing so.

7.4 Device Functional Modes

The TLV915x-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (± 1.35 V). The maximum power supply voltage for the TLV915x-Q1 is 16 V (± 8 V).

The TLV915x-Q1 S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV915x-Q1 family offers excellent DC precision and DC performance. These devices operate up to 16-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 4.5-MHz bandwidth and high output drive. These features make the TLV915x-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 Low-Side Current Measurement

图 8-1 shows the TLV9151-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in 图 8-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, [0-A to 1-A Single-Supply Low-Side Current-Sensing Solution](#).

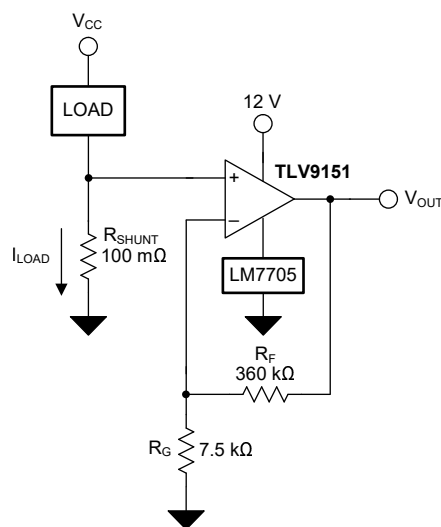


图 8-1. TLV9151-Q1 in a Low-Side, Current-Sensing Application

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in [图 8-1](#) is given in [方程式 1](#).

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using [方程式 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using [方程式 2](#), R_{SHUNT} is calculated to be 100 m Ω . The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV9151-Q1 to produce an output voltage of 0 V to 4.9 V. The gain needed by the TLV9151-Q1 to produce the necessary output voltage is calculated using [方程式 3](#).

$$\text{Gain} = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using [方程式 3](#), the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G . [方程式 4](#) is used to size the resistors, R_F and R_G , to set the gain of the TLV9151-Q1 to 49 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 360 k Ω , R_G is calculated to be 7.5 k Ω . R_F and R_G were chosen as 360 k Ω and 7.5 k Ω because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. [图 8-2](#) shows the measured transfer function of the circuit shown in [图 8-1](#).

8.2.1.3 Application Curves

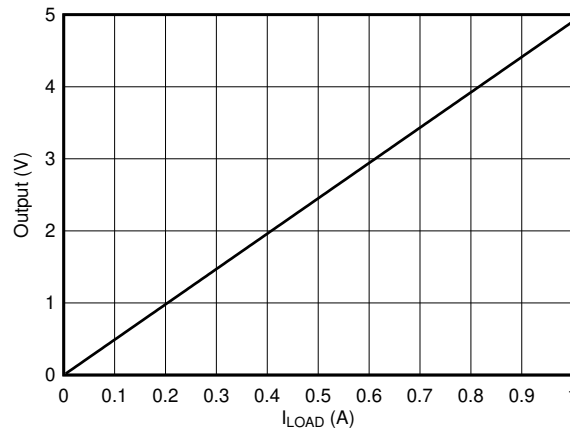


图 8-2. Low-Side, Current-Sense, Transfer Function

9 Power Supply Recommendations

The TLV915x-Q1 is specified for operation from 2.7 V to 16 V (± 1.35 V to ± 8 V); many specifications apply from -40°C to 125°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [§ 6.8](#).

CAUTION

Supply voltages larger than 16 V can permanently damage the device; see [§ 6.1](#).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to [§ 10](#).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [图 10-2](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

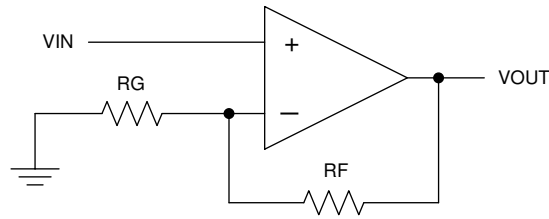


图 10-1. Schematic Representation

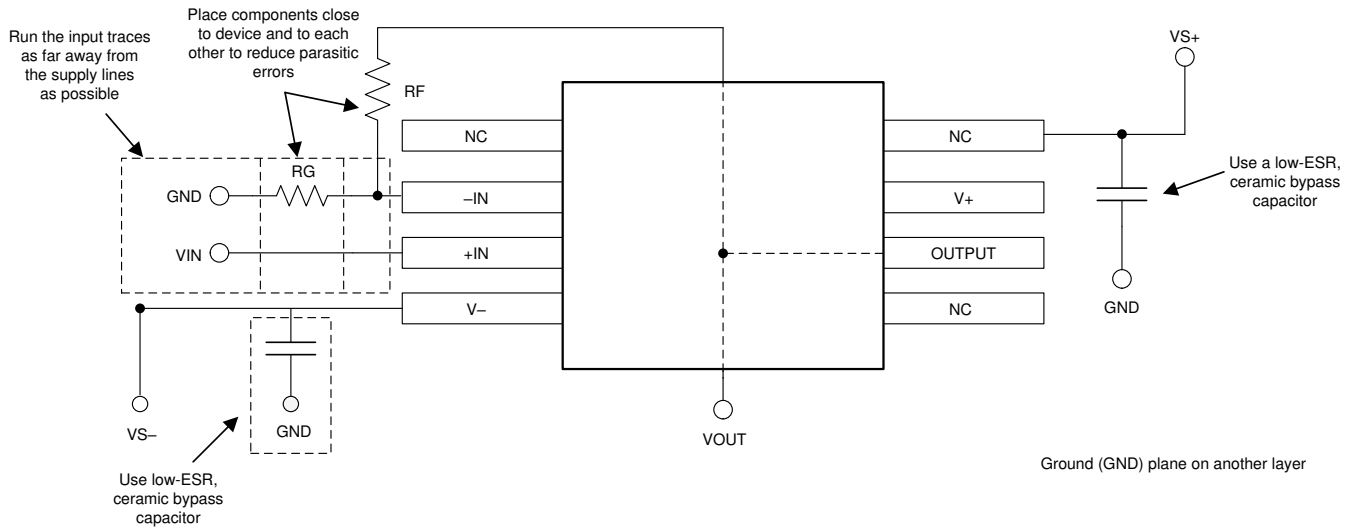


图 10-2. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

11.1.1.2 TI Precision Designs

The TLV915x-Q1 is featured in several TI Precision Designs, available online at <http://www.ti.com/ww/en/analog/precision-designs/>. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

Texas Instruments, [Analog Engineer's Circuit Cookbook: Amplifiers](#)

Texas Instruments, [AN31 amplifier circuit collection](#)

Texas Instruments, [0-A to 1-A Single-Supply Low-Side Current-Sensing Solution TI Precision Design](#)

Texas Instruments, [The EMI Rejection Ratio of Operational Amplifiers application report](#)

Texas Instruments, [Op Amps With Complementary-Pair Input Stages application note](#)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9151QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JKF	Samples
TLV9152QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27XT	Samples
TLV9152QDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9152Q	Samples
TLV9154QDRQ1	ACTIVE	SOIC	D	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9154QD	Samples
TLV9154QDYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9154Q	Samples
TLV9154QPWRQ1	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9154Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9151-Q1, TLV9152-Q1, TLV9154-Q1 :

- Catalog : [TLV9151](#), [TLV9152](#), [TLV9154](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9151QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9152QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9152QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9154QDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9154QDYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV9154QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9151QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9152QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9152QDRQ1	SOIC	D	8	3000	356.0	356.0	35.0
TLV9154QDRQ1	SOIC	D	14	3000	356.0	356.0	35.0
TLV9154QDYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV9154QPWRQ1	TSSOP	PW	14	3000	356.0	356.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

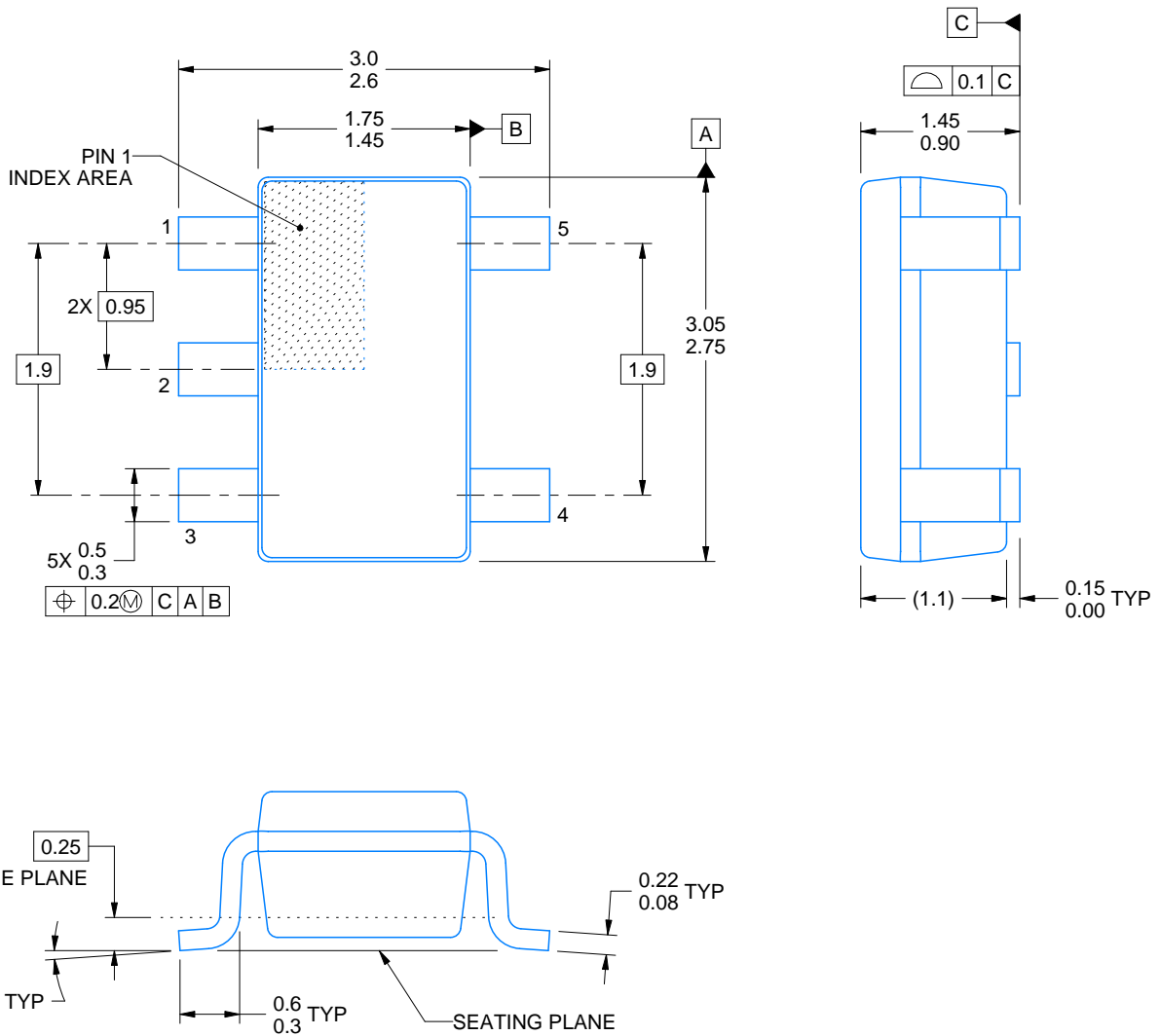
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

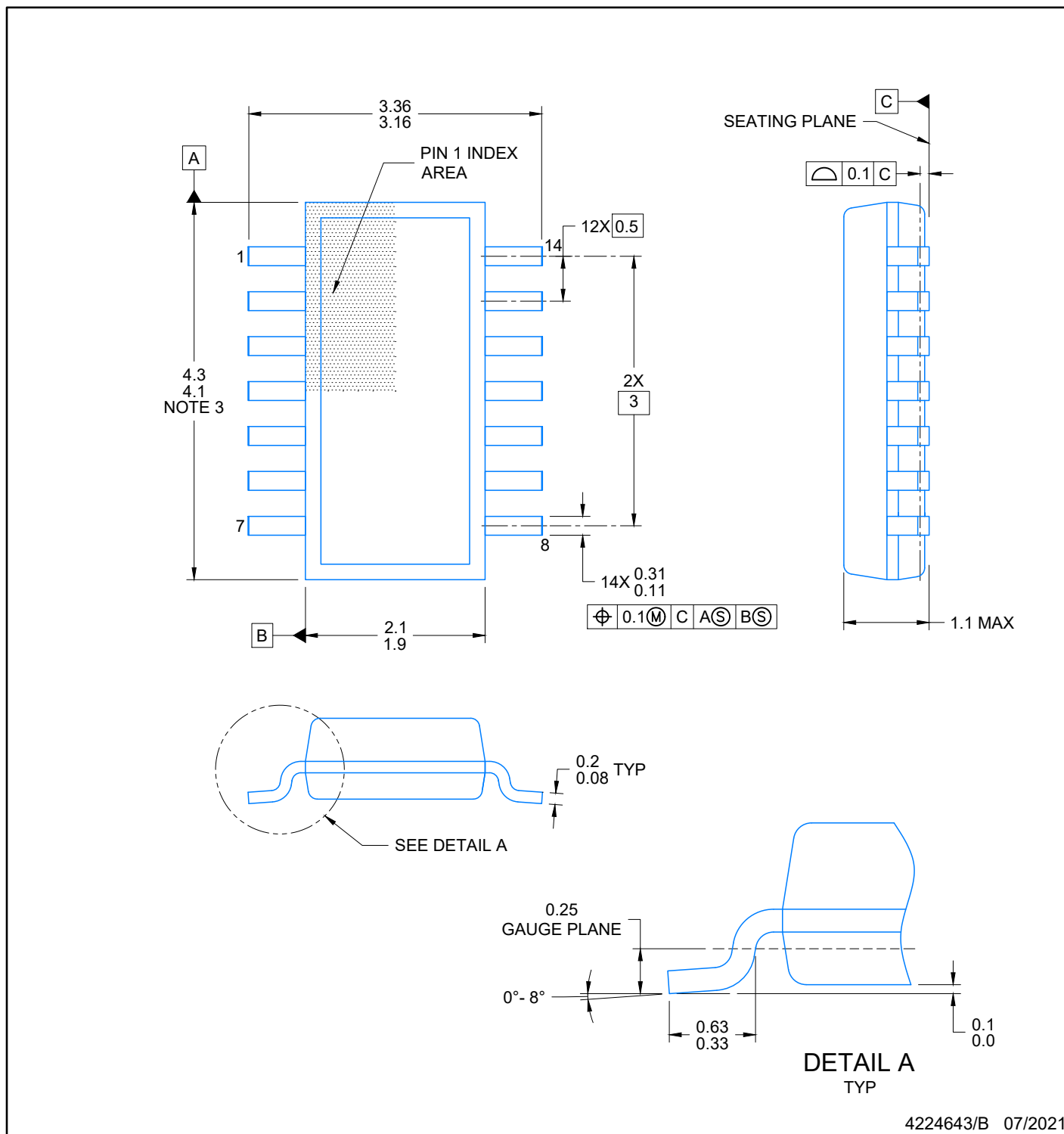


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

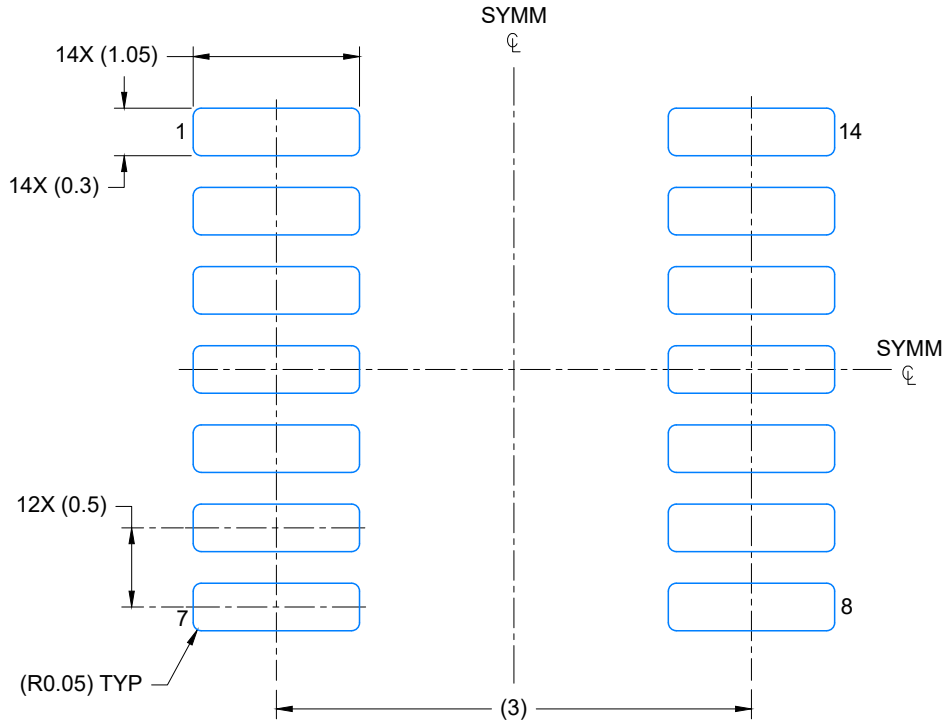
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

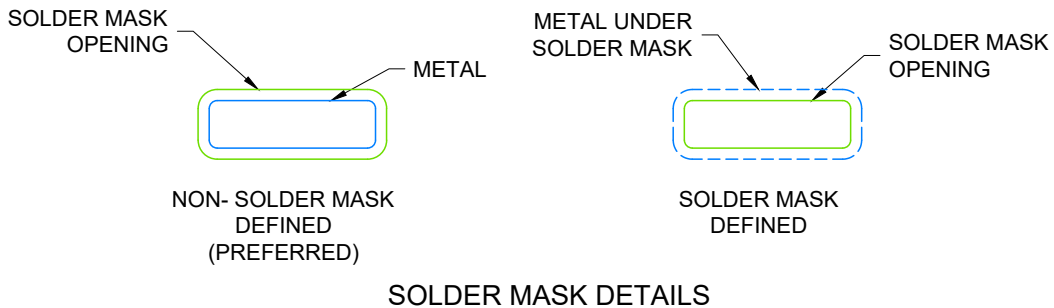


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



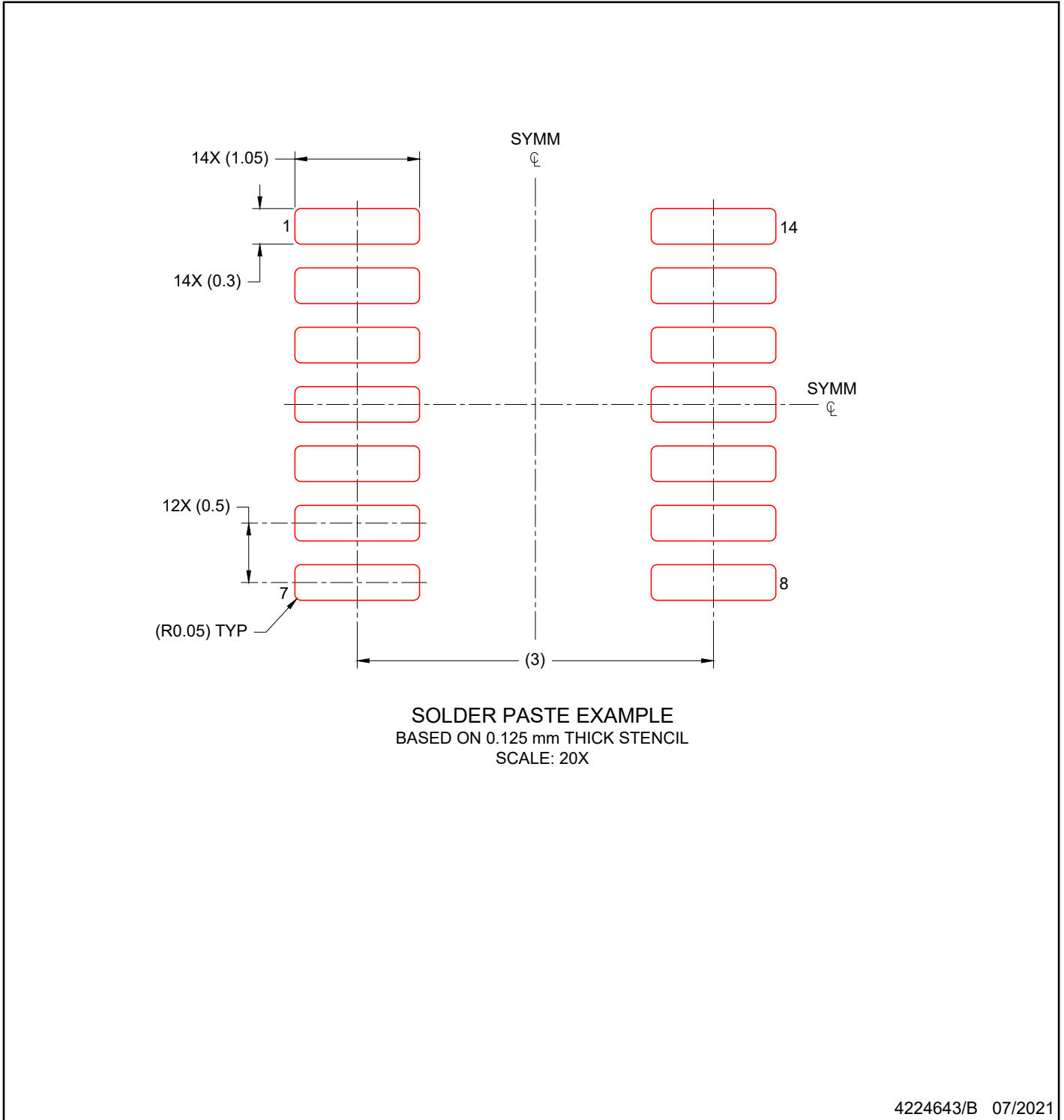
LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE: 20X



4224643/B 07/2021

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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